Negative Input Resistance and RMS Input Currents

The often unrecognized plagues of dc/dc converters

Many SMPS designers and users of modules will have been puzzled by mysterious wild oscillations and bewildered by their resistance to changes in the regulation loop. DC/DC converters suffer from negative input resistance which can cause wild oscillations and overstressing of components, especially in conjunction with input filters. Also, the high rms input currents of many configurations are often overlooked. These facts are obviously widely unknown.

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Lately, in several one-day „Seminars” about dc/dc converters, the speakers made some factually wrong statements revealing they had no notion of the existence of negative input resistance and high rms input currents. Neither during the presentations nor in the texts handed out both were mentioned. The converter input was disregarded, the choice of the capacitors arbitrary, the screen shots of the software tools lacked input parameters. This triggered a survey of seminar papers, data sheets, application notes and hundreds of magazine articles about converters from today to several decades back which yielded only 2 articles of 74 und 78 about NIR! Obviously, its existence and dangers are widely unknown.

Due to the spreading use of SMPS, many engineers from other areas of electronics venture into SMPS design, grossly underestimating the complexity. These days, too many preachers dare to run seminars and write texts about SMPS design who lack expertise and practical experience. In this context, it is noteworthy that seminar and similar texts usually present an odd 30 pages about theoretical loop design without any hint that there are other reasons for instability.

Especially some semiconductor companies are trying for years to persuade customers to dive into SMPS by insinuating all that is needed is their wonder chip, some inductor and a capacitor, and bingo, there is the SMPS! Also, there is an enormous number of modules on the market, their small size and low price deceptive, as most of them require the addition of a sizeable number of components. No data sheet mentions NIR and rms currents, warns the user that he is not free to add to the input whatever he chooses. Often „input filter” circuits are recommended which cause hefty NIR oscillations.

Professional SMPS design requires the combined and profound knowledge of DC to high frequency amplifier and regulation loop design, sampling systems, nanosecond switching and converter circuits, magnetic components and the ability to design them which also requires knowledge of ferrites, isolation and winding materials, active and passive components, c.e.board layout. A further prerequisite is proficiency in measurement technology.

Origin of NIR in dc/dc converters

By definition a positive resistance absorbs energy, a negative resistance delivers energy. The reason why NIR does not always produce wild oscillations is the prevalent use of aluminum electrolytics, at least in all higher power converters, their rather high ESR often provides enough damping. The vast number of low voltage buck converters use MLC capacitors, hence even minute stray inductances may suffice to cause oscillations, also, as will be shown, the danger rises with decreasing input voltage.

The purpose of a voltage regulator is to maintain a constant voltage across the load. Linear regulators keep the input current constant as it is identical to the output current, they present a constant-current load to the source, the input power rises linearly with increasing input voltage; the input resistance is positive; in transient situations it could become negative. Shunt regulators are constant - resistance loads, their input current rises linearly, the power with the square of the input voltage, their input resistance is positive. DC/DC converters, due to their high efficiency, nearly independent of input voltage, draw an almost constant power; this means that the input current drops with increasing input voltage.

This constitutes a negative input resistance (NIR). A general definition:

All dc/dc converters which draw constant input power for a constant load exhibit a negative input resistance resp. impedance which generates wild nonlinear oscillations unless enough damping in the input circuit is provided.

Figure 1: A buck converter with voltage regulation and an internal input capacitor. The averaged input current falls with increasing input voltage resulting in NIR.
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It is material to realize that the existence of NIR does not require an output voltage, current or power regulation loop. It is only necessary that the input power remains constant if the input voltage is changed for a constant output power. The majority of converters display NIR only if a regulation loop is present which keeps the output power constant.

To prove the point that a loop is not necessary for NIR, consider a flyback in DCM, the output power will be \( P = \frac{1}{2} \times L \times i_{\text{peak}}^2 \times f \). L and f being constant, the power depends only on the peak current with which L will be charged. If that peak current is just kept constant, this will be a constant power converter, variations of the input voltage will have no effect on the output and hence the input power, if the load is a resistor, the voltage will stay constant. This is not to be mixed up with current-mode control because there is no loop. Current-mode control incorporates a comparator fed by a current-dependent signal and the output of the voltage loop error amplifier; there are even two loops. If the charging current can be set with a potentiometer, a linear increase will cause an increase in power by the square, the voltage across a load resistor will rise linearly.

This is an entirely open loop system.

For further clarification, consider a converter with a voltage regulation loop where the gain of the error amplifier can be adjusted with a potentiometer from zero to maximum. With the gain set to zero, there is no regulation, the output voltage follows the input, hence this is a constant-resistance load to the power supply, the input resistance is positive. Then the gain is set to its maximum, now becomes a constant-power load with negative input resistance. At some finite gain, somewhere in between, the input will behave as a constant – current load, this is the point, where the input resistance will change sign; exactly at this point the input resistance will be infinity as it should be for a constant-current input. Hence the input resistance will change with increasing gain from the value of the output load towards positive infinity and come down from negative infinity to a value of negative resistance which will depend as we shall see on the input voltage and the power.

The oscillations caused by NIR have hence not necessarily something to do with the existence and operation of a voltage loop. But interactions may happen: the loop, if it is fast enough, will try to compensate for the changes in input voltage. This is best seen in a buck in CM, because the output voltage depends directly on the input voltage, any changes require a proportional change in duty cycle by the loop. The closer the resonance frequency of the input comes to the bandwidth of the loop (which must be <= 1/10 the switching frequency), the less the loop is able to compensate fast enough. The NIR changes to a negative input impedance. The interactions may become quite complex. The input resonance frequency will then also change with increasing gain from the value of the output load towards positive infinity and come down from negative infinity to a value of negative resistance which will depend as we shall see on the input voltage and the power.

Many converters draw sizeable peak and rms input currents, e.g. the simple buck. With bucks, the rms current depends on the operation mode, DCM or CM, it is safe to always use the formula \( \text{rms} = \frac{i_{\text{peak}}}{\sqrt{2}} \times \sqrt{\text{D}} \) since these currents sport also very short rise and fall times, they are awkward loads for the source, so a good capacitor at the input is mandatory in the first place; but this may not suffice, so often an input LC filter is inserted. This can play havoc with the system as will be shown, this means asking for trouble! This can not only create strong wild oscillations but also overstressing of components.

Explanation of NIR

The designation „NIR“ is not well chosen because it is not – like a resistor – a real component, but it describes the behavior or the property of an operating electronic circuit; if the supply is switched off, the NIR disappears. It can be measured with suitable instruments by placing a resistor in parallel which overcompensates the NIR, by subtracting its value from the result, the value of the NIR is obtained.

NIR resp. impedance is by no means new, designers of wide band amplifiers are familiar with this effect since decades, presumably since the 30’s. Any emitter follower displays a negative input impedance. This comes about because energy is fed back from the output (emitter) to the input (base) via the base-emitter capacitance, this is a simplified explanation. If there is a resonant circuit in the input, the circuit will oscillate. A capacitance is always present, hence a minute amount of conductor inductance is sufficient to produce very high frequency oscillations. Of the 3 methods of compensation one can be used with dc/dc converters. In oscillators NIR is desired to overcompensate the losses.

In most cases, a NIR is highly undesirable because it either disturbs the operation of a circuit or renders due operation impossible. NIR means that energy is delivered, often in reverse like in this case. The notion that the input of a power supply can deliver energy may not easily come to mind, in fact NIR may be visualized as a negative current coming out of the input. The wild oscillations can easily be mistaken for regulation loop instability because almost all papers about converters know no other cause. As we shall see, the NIR is highly nonlinear, hence the oscillations are nonlinear and may only occur in certain input voltage/load configurations.

If the designer is not familiar with NIR and did not test all combinations, a SMPS design may well go into production, and the problems show up later. Testing is not enough, though, because calculations have to prove that even a worst case combination of tolerances cannot lead to oscillations.

A numeric example

NIR can best be visualized by a numeric example: consider a voltage source with an internal resistance of 1 ohm; first it supplies power to a resistor and then to the input of a converter, in both cases the output power is assumed to be 4 W.

In the first case a simple voltage divider results: if the source voltage rises, will the current, the voltage drop across \( R_i \) will rise, the source’s power by the square.

In the second case the input current will generate an initial voltage drop across the internal resistance \( R_i \), the converter input voltage will be \( V_{\text{in}} = V_S - V_{R_i} \). If the source voltage rises, the input current will drop, hence the voltage drop across \( R_i \) will be reduced. This increases the actual input voltage further, so the input current will drop still more and so on, until a stable state is reached. The regenerative nature is already apparent. The following table shows all parameters for 4 values of input voltage:

<table>
<thead>
<tr>
<th>( V_S )</th>
<th>( I_S )</th>
<th>( V_{R_i} )</th>
<th>( P_{\text{in}} )</th>
<th>( V_{\text{in}} )</th>
<th>% of ( V_S )</th>
<th>( P_{\text{out}} )</th>
<th>( P_{\text{out}} - R_{R_i} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 V</td>
<td>1.6 A</td>
<td>1.6 V</td>
<td>2.56 W</td>
<td>2.4 V</td>
<td>60 %</td>
<td>4 W</td>
<td>1.4 ohms</td>
</tr>
<tr>
<td>5 V</td>
<td>1 A</td>
<td>1 V</td>
<td>2.5 W</td>
<td>4 V</td>
<td>80 %</td>
<td>4 W</td>
<td>4 ohms</td>
</tr>
<tr>
<td>10 V</td>
<td>0.42 A</td>
<td>0.42 V</td>
<td>0.18 W</td>
<td>9.6 V</td>
<td>96 %</td>
<td>4 W</td>
<td>23 ohms</td>
</tr>
<tr>
<td>20 V</td>
<td>0.2 A</td>
<td>0.2 V</td>
<td>0.04 W</td>
<td>19.8 V</td>
<td>99 %</td>
<td>4 W</td>
<td>98 ohms</td>
</tr>
</tbody>
</table>

Table 1: Parameters for values of input voltages
The NIR shows up readily in these parameters:

1. The power lost in the internal resistance $P_{int}$: it drops with increasing source voltage from 2.56 to 0.04 W, because the current drops. If there were a positive input resistance, the power lost would rise with the square of the current.

2. The power delivered by the source: it drops with increasing voltage from 6.4 to 4 W. If there were a positive input resistance, it would rise with the square.

3. The percentage of the source voltage which arrives at the input, it increases fast from 60 to 99 %. If there were a positive input resistance, this would constitute a voltage divider, i.e., the percentage would remain constant.

4. Clearly, the problem becomes worse for low input voltages and high currents resp. powers, NIR decreases, so the damping becomes more difficult. The message is to use a high input voltage if that choice exists.

If $R_i$ is increased from 1 to 1.5 ohms, the $-R_i$ values change to $-2.6$ ohms at 5 V, $-22.1$ ohms at 10 V, $-97$ ohms at 20 V. The reason is that due to the higher voltage drops across $R_i$, the input voltages drop which in turn causes higher input currents which eventually result in still lower NIR values. Here $-R_{in} = +V_{in}/-I_{in}$, this means that, for each stable operating point, the input behaves like a fictitious resistance of that respective value. As shown later, it is a dynamic resistance. The larger $R_i$ becomes, the worse the problem gets. It is now immediately obvious that a series inductance between source and input is fatal, as it acts as a high impedance for any current change. The logic consequence is that an input capacitor is mandatory which can deliver resp. absorb current spikes. This completes a resonance circuit, and it is again apparent that the input will oscillate if the equivalent parallel damping resistance at the input is greater than $| -R_{in} |$. If an “input filter” is added which includes a fairly high amount of inductance, it can not surprise that oscillations are provoked.

There is no way around performing the calculations following, including tolerances and extremes of operating conditions and to test engineering models thoroughly for critical combinations. During oscillations, voltages and currents can easily reach destructive levels which is especially dangerous with today’s low voltage active and passive components. Many ic’s are destroyed already above a few volts, one spike can be sufficient.

Calculation of NIR. Input resonance circuit

There are two input resonance circuit configurations: 1. The resonance circuit where the inductance is undesired, it consists of the sum of conductor inductance, source inductance, capacitor ESL. 2. An input filter.

Whether oscillations are sustained or not depends on the quality factor Q, i.e. the ratio L/C resp. (L/C)/R. A high L/C ratio denotes a high impedance circuit and vice versa. If Q is high enough, the impedance will peak at the resonance frequency $1/(2\pi \sqrt{LC})$. In order to achieve sufficient damping, with given values of L and C, the damping resistance must stay below resp. exceed a maximum/minimum value, depending on whether it is defined as a parallel or series resistance. With aluminum electrolytics, this is often fulfilled by the ESR if only conductor parasitic inductance and ESL are present. Consequently, an ideal capacitor like a MLC type is out of place at the input, but mostly specified for low voltage bucks these days. The trouble is that the oscillations show up strongly in the input current = capacitor current, not so spectacular in the input voltage depending on the capacitance value and type. The current is difficult to measure in SMD circuits. It is hence wrong to assume that lower ESR is always better, this is also true at the converter output as well. It is now evident that capacitors should be placed close to the regulators resp. converters, also for completing the hf circuits. It should be borne in mind that the ESR decreases sharply with rising temperature, hence a converter may remain quiet at room temperature and start to oscillate when it warms up! Also it may only oscillate with high currents i.e. high powers. Regarding aluminum capacitors, the matter is further complicated by the fact that for stability a minimum ESR is necessary while the manufacturers only specify a maximum value at 25°C, they may deliver arbitrarily lower values. Hence a professionally designed circuit cannot rely on capacitor ESR!

NIR is not constant and highly nonlinear. For modern SMPS it can be assumed that the efficiency is almost independent of the input voltage and high, hence the input power will also be independent of the input voltage. Under these assumptions it follows:

$$ R_{in} = 1/(di/dv) = -V_i^2 / P_i = -P_i / I_i^2 $$

It depends hence on the square of the input voltage, with respect to the current it follows a hyperbola $1/x^2$. If the choice exists, one will select a high input voltage. And the danger rises with decreasing input voltage. A high input voltage with an associated low current is equivalent to a high input resistance, and vice versa. The most critical combination is lowest input voltage together with the highest load; this is equivalent to a generator with a low internal resistance which can deliver a high current into the resonance circuit.

A brief survey of the formulas for a parallel resonance circuit: The impedance at the resonance frequency

$$ 1/(2\pi \sqrt{LC}) $$

is: $Z_{max} = (L/C)/R_s$

The quality factor

$$ Q = (2\pi f L)/R_s, \ R_s \ is \ the \ series \ damping \ resistance. $$

$$ = R_p/(2\pi f L), \ R_p \ is \ the \ parallel \ damping \ resistance $$

$$ = 2\pi f C R_s = 1/(2\pi f C R_s), \ R_s = ESR $$

$$ = 1/d, \ d \ = \ damping \ factor $$

It is immaterial whether the damping resistance is in series with the inductance or the capacitance, the damping rises with increasing resistance. Q decreases with rising capacitance. The lower L/C, the lower Z. It follows that maximum damping is achieved if L/C is kept as low as possible and $R_s$ as high as possible.

There is hence a parallel combination of the Z of the resonance circuit and the input resistance of the converter. For parallel circuits the conductances are added, their sum inverted:

$$ R_{eff} = 1/(1/Z + 1/R_{in}) $$

Oscillations at the resonance frequency will occur if the condition for oscillation is fulfilled:

$$ \text{Reff} < 0 \ \text{resp.} \ Z = (L/C)/R_s > R_{in} $$
Expressed differently, the

**Condition for stability:** \( \frac{L/C}{R_s} < R_{in} \)

must be fulfilled. If the converter, input voltage, and load are given, instability can only be avoided by decreasing \( Q \) resp. \( L/C \) or/and increasing the series damping resistances resp. decreasing the parallel damping resistances.

When the sum of the series resistances \( R_{Series} = R_{Source} + R_L + R_{Conductors} \) can not be neglected, the formula can be extended; no oscillations will occur if the inequality:

\[
R_E = \eta \frac{V_i^2}{P_i} > \left( \frac{L/C + R_{Series} R_C}{(R_{Series} + R_C)} \right)
\]

is fulfilled. For \( R_{Series} = 0 \) the expression shrinks to the one above.

As \( R_{in} \) depends on \( V_i^2 \), the system is nonlinear, hence oscillations will not be sinusoidal, but strongly distorted. \( L \) may be current-dependent and \( C \) voltage-dependent which complicates the situation. In case the resonance frequency comes close to the bandwidth of the regulation loop, an inductive component is added to the input resistance such that it becomes an input impedance, due to the lagging response. If the frequency of the \( V_i \) and \( P_i \) changes is above the bandwidth of the loop, further complications arise because heat frequencies with the switching frequency are possible which can cause irregular behaviour.

**A professional compensation method:**
As outlined before, it is not acceptable that the damping is based on such an unreliable and drifting parameter as capacitor ESR. Adding resistance in series with a high value capacitor would entail undesirable losses. A method used in wideband amplifier design fulfills the purpose without incurring disadvantages: A high quality capacitor such as a MLC or stacked polyester type is connected in series with a non-inductive damping resistor calculated according to the formulas above and placed in parallel to the input (and the high value capacitor which is mostly an electrolytic). The capacitance needed is very low (tenth of \( \mu F \) to a few \( \mu F \)) because the frequencies to be damped are high. This RC combination ensures sufficient damping which is independent of temperature, voltage and age. It has to be placed directly at the converter input, the position of the other capacitor is less critical, but the high current conductor routing has to be correct. At first sight, a parallel circuit of this resistor and the ESR seems to exist, but this is not true: high currents always seek the loop of minimum impedance resp. inductance, this is through that RC combination, all other loops show higher impedance due to conductor inductance and ESL. This method is also applicable to the outputs of converters and low-drop linear regulators.

**Summary of the methods of avoiding/compensating NIR:**
Without exception, there must be a sufficiently large capacitance at the input of each regulator, whether linear or dc/dc converter. As most converters draw high rms currents, the capacitor must be adequately sized.

1. Input voltage as high as possible if that option exists.
2. Low \( Q \), i.e. \( L \) small, \( C \) large. This implies placement of capacitors close to the input, low inductance conductor routing, minimizing of conductor loop area.
3. High efficiency reduces input power and improves the NIR.
4. Use of the compensation method in Fig. 3.

5. The selection of input capacitors.
Still many 2012 texts recommend „solid tantalum” as the „best” capacitors for converter inputs and outputs which is wrong for several reasons: their low ESR is undesirable at inputs and outputs, their data sheets prescribe a minimum of 3 ohms per volt impedance which rules them out across power supplies, their reliability is poor and they usually short out and burn. Their manufacturers hence prescribe fuses to disconnect shorted tantalums. Meanwhile there are better components like polymer types and such of different materials like Niob. The same holds true for „MLCC”, they are excellent regarding their low ESR and ac current capability, but exactly this can cause severe wild oscillations, due to NIR at the input or loop oscillations at the output. Also, those texts never check whether these capacitors can at all take the high ac currents; the suppliers mostly give only a dissipation factor taken at 1 KHz and 1 Vrms which is hardly descriptive of the application in converters. Also, MLC capacitors are recommended without the warning, given in every data sheet of the Japanese manufacturers, that they should not be stressed beyond half the rated voltage! Larger SMD types are prone to bakeage and then burn up.

A 48 W – 60 V – 700 mA LED module of an Eastern Asian manufacturer was tested. An input circuit was prescribed which consisted of: 2 x 4.7 \( \mu F \), a 47 \( \mu H \) inductor in series and a 330 \( \mu F/100 \) V electrolytic at the converter input. Strong NIR oscillations arose which, as expected, depended heavily on the operating point.
With 48 V and a 14.5 W load an average input current of 0.31 A was measured, but at the converter input a rms input current of 0.36 A flowed, also through the 330 uF. Fig. 4 shows the input current and the output voltage ripple. A 330 uF is typically specified for 0.66 to 0.78 Arms, so the size of the 330 uF/100 V was dictated by the ripple current rating with a margin of 50 %.

In another operating point the total peak-to-peak current even amounted to ~ 0.12 A to + 0.85 A = 0.92 App. In order to prove that these high peak and rms currents were caused by NIR and the prescribed input circuit, the 330 uF was removed and a RC combination of a 1 uF low-inductance stacked mylar cap and a 10 ohm resistor was placed across the input: the pp current shrunk from 920 to 20 mA, the rms current from 360 to 7 mA! The average input current from the source stayed almost constant. The 47 uH series inductor and the 2 x 4.7 uF input capacitors were still in the circuit.

![Image of converter input current with RC damping](image)

Figure 5: With RC damping: input current, above, same scale 0.1 A/cm, zero at the bottom, and output voltage, 110 mVpp, 100 mV/cm. The residual current ripple is hardly visible.

Figure 5 shows the converter input current with the RC damping. Obviously there is and never was a need for the big 330 uF/100 V electrolytic, it provoked the oscillation and the high peak and rms currents, also by its ESL. The series inductor was later reduced from 47 to 2.2 uH, the voltage ripple at the input was a mere 0.16 Vpp on the 48 V dc. The stacked mylar capacitor could be replaced by a smaller MLCC of 1 uF/100 V X7R. The internal circuit of the module is unknown, also whether there is an input capacitor. When the series damping resistor was reduced, the propensity to oscillations rose, eventually they started again.


The faster the circuits become and the smaller, the worse the measurement problems! Looking at the recommendations given in most recent papers about converters, the expert is shocked! Here at least some important directions.

1. Measurements with voltage probes in fast circuits are only meaningful if Tektronix probe adapters are used in which all 5 mm probes fit. They are available as screw-in (no. 131-0258-00) and solder-in (no.131-4353-00) versions. They are soldered directly on top of the respective capacitor, the probe is then inserted, the “ground cable” taken off. This is also the only way to prevent stray magnetic fields from transformers etc. to couple into the loop of the ground lead and cause – often totally – erroneous readings. Alternatively, the special tiny probes for SMD components can be used. The voltage probes must be compatible with the scope inputs, their up to 6 hf adjustments must be carefully adjusted to the input used, for this purpose a pulse generator with a rise time of < 1 ns and a clean top and a special probe-to-BNC adapter (no. 013-0085-02) with a 50 ohm feedthrough termination (e.g. Suhner) are required. If this was not performed, no accurate measurements can be expected. Due to the low maximum voltage specs of most modern active components, it is vital to measure overshoots etc. precisely. The most recent active power components, SiC and GaN JFETs, have no avalanche rating!

Many convertors operate at high frequencies up into the MHz range. It has to be borne in mind that passive voltage probes have very low input impedances at high frequencies, down to a few hundred ohms; the „10 Mohms/10 pF“ are valid only to appr. 100 KHz. This means that hf circuits can be affected by contacting a probe, overshoots damped. If this danger exists, active FET probes must be used.

2. In all SMPS designs, a current probe is absolutely indispensable, otherwise the designer remains blind. The DC/AC probe is the proper choice. The AC probes are faster, but they are saturated by dc components and hence rarely usable in SMPS. E.c. board traces have to be cut, a short loop made of hf litz wire is soldered to the ends, both wires run as a strand for as long as is necessary to insert the probe into the loop. The probe must not lie close to inductive components as it might pick up stray fields. The probe has an insertion impedance which may disturb very low impedance circuits. A practical difficulty arises e.g. in dense layouts, when one or more input chip capacitors are directly at the ic pins and there are large copper areas which cannot be cut. Here, the only means is to lift the chip capacitor or the ic pin off the board on one side and solder the loop in between. NB: current probes are always inserted at the ac low end. However, it is feasible to even place the loop in the drain lead of a flyback transistor; there may be some capacitative feed through, though.

There are also various current sensors available which do not require cutting conductors, some are shaped like a pencil and carry a tiny magnetic field sensor in the tip which is just placed upon the conductor; with some effort it can even allow calibrated measurements. The bandwidth is only 5 MHz, but this is mostly sufficient to detect currents, and it is quick.

Wild NIR oscillations will be mainly visible in the input current; depending on the size and quality of the input capacitor and its placement, the voltage amplitude may be fairly low and misleading. If the value of the NIR is very low, then the insertion of the probe may influence the oscillation.

3. Digital Storage Oscilloscopes (DSO’s) do not show the signal, but a more or less distorted reconstruction, and their sampling rates and bandwidths are NOT constant. The actual sampling rate depends on the memory and the sweep speed selected, irrespective of the maximum value. The low and middle priced models mostly have only small memories from 1 to 10 KB; this means in practice, that even a 5 GS/s 500 MHz DSO, at a slow sweep speed for showing mains-related signals, may have only 50 KS/s left! The bandwidth is only 1/10 (not 1/2!) of the sampling rate, hence the 500 MHz shrink to 5 KHz! Of course, this does not appear in advertisements or manuals, but is plainly admitted in other publications of the manufacturers. If the sampling rate is insufficient, all kinds of distortions and artefacts can be displayed which have no resemblance to the signal. For most work on SMPS analog scopes are vastly superior, for elementary physical reasons, they cannot display false signals, and they display the signal itself. Of course, if a DSO shows artefacts, all numeric displays are false. 

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