Residue-free room temperature UV-nanoimprinting of submicron organic thin film transistors


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In this study we report on an innovative nanoimprint process for the fabrication of entirely patterned submicron OTFTs in a bottom-gate configuration. The method is based on UVNanoimprint Lithography (UV-NIL) combined with a novel imprint resist whose outstanding chemical and physical properties are responsible for the excellent results in structure transfer. In combination with a pretreated stamp the UV-curable resist enables residue-free imprinting thus making etching obsolete. A subsequent lift-off can be done with water. The UV-NIL process implies no extra temperature budget, is time saving due to short curing times, eco-friendly due to a water-based lift-off, simple because it is etch-free and completely r2r compatible. It works perfectly even if ultra-thin organic and hybrid films are used as gate dielectrics. On this basis entirely patterned functional submicron OTFTs with pentacene as the semiconductor are fabricated showing clear saturation, low switch-on voltage (~3 V) and a sufficiently high on-off ratio (10^3).

1. Introduction

The success of more demanding organic electronic applications such as high data rate RFID tags, fast sensor networks, large memories, wearable computers and sensors depends on a multiplicity of performance parameters of the involved circuits [1–4]. First and foremost these are the switching speed, the integration density, the driving voltage, and the fabrication yield of the circuits. As smaller devices are faster, require lower driving voltages, allow for higher integration densities and, due to their smaller active areas, have smaller gate leakage currents, there is a major drive to decrease the critical dimensions of organic thin film transistors (OTFT).

Over the recent years Nanoimprint Lithography (NIL) has become a serious alternative for high-resolution patterning of organic electronic devices in an in-line manufacturing environment. Photolithography is not likely to become a very low-cost roll-to-roll (r2r) process and in volume printing techniques with minimum feature sizes of 20 μm a resolution in the submicron region is clearly out of reach [5,6]. NIL is on the one hand suitable for r2r-processing and on the other hand it provides an excellent...
spatial resolution, which to date is limited only by tool-making capabilities. Apart from its unrivalled high-resolution, NIL has several more advantages over competing patterning methods such as self-aligned ink-jet printing [7] or high-resolution ink-jet printing [8]. It allows a higher aspect ratio, a larger number of compatible materials, a shorter process times which is inherent to parallel structuring techniques and an easier implementation into a standard r2r facility [9,10].

Hot Embossing is the oldest NIL technique and has already proven to be applicable in defining sub-micrometer channel lengths of OTFTs based on rigid silicon substrates [11,26] as well as of entirely patterned OTFTs based on thin organic gate dielectrics and on polyester film substrates [13]. However, in the latter case Hot Embossing can be detrimental to the fabrication process of large circuits since it often requires a temperature surpassing the glass transition temperature of the duroplastic films, thereby generating dimensional instabilities and complicated registration. Furthermore, Hot Embossing always produces a residual layer of the thermoplastic resist which has to be removed by anisotropic etching. This etching process is particularly undesirable because it is costly, difficult to control and might be harmful for an organic layer underneath.

In an alternative approach – UV-Nanoimprint Lithography (UV-NIL) – the thermoelastic imprint resist is replaced by a UV-curable polymer, bringing about several advantages in comparison to Hot Embossing. With UV-NIL, pressure, process time and thermal stress for the substrate can be significantly reduced during imprinting. Due to the major advances in nanometre patterning along with low-cost and high throughput [14], substantial work has been put into the development of suitable UV-curable polymer materials [15–17]. Today, a large number of UV-NIL resists are commercially available such as Amonil-MMS4 by AMO GmbH or mr-UVCur06 by micro resist technology GmbH. So far, none of them enables both residue-free imprinting and a lift-off process by a sufficiently gentle solvent.

Here we report on a novel nanoimprint process for the fabrication of entirely patterned submicron OTFTs in a bottom-gate configuration. This process requires no extra temperature budget, imprints residue-free thereby rendering etching obsolete, is time saving due to short curing times, eco-friendly due to a water-based lift-off and fully r2r compatible. This method is based on UV-NIL combined with a novel imprint resist whose outstanding chemical and physical properties are responsible for the excellent results in structure transfer to both rigid and flexible substrates. It is shown that the UV-NIL technique works perfectly even when ultra-thin organic and hybrid films are used as gate dielectrics. Employing this method, functional submicron pentacene-based OTFTs are fabricated, which show good saturation of the drain currents, low switch-on voltage (≈3 V) and a sufficient on–off ratio (105) of the drain current.

2. Materials and methods

We have fabricated submicron coplanar OTFTs with pentacene as the active layer and a bilayer of about 100 nm of a benzocyclobutene derivative (BCB) and 30 nm of poly(vinyl cyanimate) (PVCi) as the gate dielectric. All devices have a channel width to length ratio (W/L) of 50. The aluminum gate electrodes are fabricated on a pre-cleaned glass substrate by a combination of a photolithographic process, e-beam evaporation of a 45 nm thick metal layer and a lift-off procedure using acetone as the solvent. The BCB layer is applied onto the aluminum gate electrodes by spin coating 0.33 wt.% of XU 71918 (Dow Chemicals) dissolved in 1,3,5-trimethylbenzene (Aldrich). The layer is crosslinked at 290 °C for 60 s on a hotplate. The PVCi layer (Aldrich) is fabricated by spin coating a solution of 0.2 wt.% of PVCi in chloroform at 2000 rpm. It is prebaked for 5 min at 80 °C to remove the solvent and UV-crosslinked for 60 min at 254 nm with a Benda NU-72 KM UV-lamp in inert atmosphere.

The thickness and optical constants of the dielectric layers are determined by ellipsometry based on a variable angle spectroscopic ellipsometer (VASE, J.A. Woollam Inc). The layer thickness is determined by fitting the ellipsometry data employing a simple Cauchy-model for the refractive index to be 29–31 nm for PVCi and 97 nm for BCB [18].

The silicon imprint stamp is patterned by electron beam lithography. The resist structures are permanently transferred to the silicon stamp by reactive ion etching (SF6–Ar) resulting in a final depth of about 1 µm. After stripping, an anti-sticking layer (perfluorohexyl–trichlorosilane) is applied to the stamp.

The UV-NIL-resist ACMO is fabricated by a mixture of GENOCURE® LTM and ACMO (acryloyl morpholine, both by Rahn AG) and chloroform at a mass ratio of 1:20:400, yielding a low-viscous material. Spin coating at 2000 rpm results in a homogeneous layer with a thickness of 600 nm. Curing is performed through UV exposure at 365 nm for a maximum time of 2 min. The UV-NIL structuring of the gold source–drain electrodes is done in an EVG 620 mask-aligner. A 30 nm thick gold layer is deposited by either e-beam or thermal evaporation. The lift-off is performed by dissolving the UV-resist with deionized water.

The 40 nm thick pentacene layer is thermally evaporated onto the sample in high-vacuum conditions at a rate of 0.2 nm/min for the first 5 nm and 0.8 nm/min for the remaining 35 nm.

Prior to the focused ion beam/scanning electron microscopy (FIB/SEM) investigations the specimens are covered with a 20 nm carbon layer to minimize charging of the sample. In the focused ion beam instrument Pt layers are grown by electron beam induced deposition (EBID) followed by ion beam assisted deposition (IBAD). These Pt layers protect the surface against incoming Ga ions during the cutting out and milling of the lamellas. The lamellas are transferred to a transmission electron microscopy (TEM) grid and thinned down to several tens of nanometre.

The TEM investigations are performed using a Philips CM20 (S)TEM (twins lens) with a thermionic LaB₆ cathode operated at 200 kV equipped with a Gatan Imaging Filter (GIF 200). For energy dispersive X-ray spectroscopy an HPGe detector (Noran/Thermo Fisher Scientific) employing Noran System Six software is used. Electron energy loss spectroscopy (EELS) and energy filtered TEM (EFTEM) are performed using a Gatan Imaging Filter (GIF) with a
1024 × 1024 CCD (YAG scintillator) attached to the microscope. Elemental maps were calculated using the three-window-technique.

3. Results and discussion

3.1. Imprint resist

The key component of our UV-NIL process for the patterning of submicron-spaced source and drain electrodes is an imprint resist called UV-NIL-ACMO, which is based on an acryloyl morpholine monomer (ACMO). It is curable by UV-initiated radical polymerization, is soluble in water, and shows a low viscosity. The actually applied special formulation of UV-NIL-ACMO is composed of ACMO mixed with a photoinitiator blend (GENOCURE) and highly diluted in chloroform, resulting in a low viscosity.

Acryloyl morpholine (for the chemical formula see Fig. 1a) is perfectly matches our NIL processes requirements for a variety of reasons: It provides removability by a lift-off process due to the lack of functional groups that could crosslink during polymerization, thereby preventing its solubility. Furthermore, the lift-off process can be accomplished with water as a cheap and eco-friendly solvent because of similarities in the polarity of the functional side group (morpholine) and the solvent water.

3.2. Residue-free UV-Nanoimprint Lithography

The principle of the UV-NIL process is illustrated in Fig. 2a. The first step (A) is to align the silicon stamp, which contains the elevated source–drain electrode pattern, with respect to the gate electrode. This is done in a mask-aligner. The aligned stamp is pressed into the low-viscous resist at low pressure, displacing the resist underneath the source–drain structures (B). A novelty here is the etch-free process enabled by residue-free displacement of the UV-NIL-ACMO resist due to the high difference in polarity of resist and stamp. Curing is performed by UV exposure for up to 2 min, depending on the initiator concentration, during which the source–drain pattern is permanently transferred into the resist. After removing the stamp (C) the source–drain material – in the present case gold – is evaporated onto the device (D). The subsequent lift-off is performed by dissolving the resist with deionized water; the evaporated gold layer on top of the resist is removed while the imprinted areas are preserved (E). An optical microscope image of the source–drain structures after the lift-off step is shown in Fig. 2b illustrating the complete transfer of the stamp’s source–drain pattern into the gold layer. The lift-off works perfectly for the complete electrode pattern and even for the large contact pads. Finally the active semiconductor material, here pentacene, is evaporated thus finalizing the transistor structure (F). In Fig. 2c an AFM phase signal of the pentacene layer on top of the contacts and the channel is displayed. The difference in morphology is distinctive: small (<200 nm) grains are formed on the gold layer, whereas terraced crystalline grains with a maximum size of about one micron are observed on the gate dielectric in the channel. Such a pentacene grain size is reasonable for an rms-roughness of the BCB/PVCi layer of approximately 0.4 nm [19–21].

The residue-free imprint is facilitated by the use of the aforementioned water-soluble low viscosity UV-NIL-ACMO resist in combination with an adjustment of the stamp’s surface energy to maximize the contact angle. In order to minimize the polarity of the silicon stamp it was rinsed with perfluorchloroctyl-trichlorosilane.

Contact angle measurements of the UV-NIL-ACMO resist and water on the modified silicon stamp reveal that the contact angle of the imprint resist on the modified stamp is very high (82°, see Fig. 1b) and approaches that
of water on the modified silicon stamp (100\°C176, see Fig. 1c). In addition to the low resist viscosity we suggest that a large difference in the polarity of the modified silicon stamp (non-polar) and the resist (polar) is an important factor for the absence of a residual layer.

In order to characterize the individual layers of the transistor devices the specimens were investigated by transmission electron microscopy (TEM). Cross section lamellas of the samples were prepared using a focused ion beam instrument (FIB, compare Fig. 3a inset) [22]. Fig. 3 shows a sample after the imprint step. SEM images of the lamella and its cutout are shown in Fig. 3a and the inset, respectively. The organic layers are clearly observed as dark areas in-between the glass substrate and the platinum layers used for sample protection during FIB-cutting. The image gives an overview of the appearance of the imprinted troughs for the electrodes and the resist in the center as a placeholder for the channel. A more detailed view is presented in Fig. 3b, it is a TEM bright field image showing one edge of the resist in the channel. The glass substrate, the aluminum electrode and the organic layers can clearly be distinguished. The three involved polymer layers BCB, PVCi and UV-NIL-ACMO appear as a single layer. However, since their elemental composition is distinctly different, the layers can be identified by analytical methods such as electron energy loss spectroscopy.

Fig. 2. (a) Scheme of the residue-free UV-NIL process: A silicon stamp containing the source–drain structures is aligned with respect to the gate electrodes of a resist-coated substrate (A). The stamp is pressed into the resist, thereby completely displacing the resist below the source–drain structures (B). Subsequently the resist is cured by UV exposure. After the stamp removal (C) the source–drain material is evaporated onto the substrate (D). The imprint resist is dissolved with water which leaves the metal source–drain electrodes well preserved (E). Finally the sample is covered by an organic active layer, pentacene. (b) Optical microscope image of the gold source–drain pattern of a submicron OTFT with L = 950 nm after lift-off. (c) AFM phase image (5 × 5 μm) of the pentacene layer formed on top of the contacts and in the submicron channel. The gate dielectric is BCB/PVCl.

Fig. 3. A sample after the imprint step. (a) A cross section lamella of the sample, where the imprinted organic layer appears dark in-between the glass and protective Pt layers. The lift out of the FIB prepared lamella is seen in the inset. (b) A TEM bright field image of the edge of the channel. (c) Superposition of EELS elemental maps (N = green; Si = blue; C = red; Al = white) enables a clear distinction of the three involved polymers. The white arrow points towards a bump in the imprinted area which is identified as PVCi. A UV-resist residual can be excluded. IBAD = ion beam assisted deposition, EBID = electron beam induced deposition. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)
BCB can be identified by its silicon content and UV-NIL-ACMO by its nitrogen content. A superposition of elemental maps of different elements is shown in Fig. 3c, where the nitrogen map is green (representing UV-NIL-ACMO), the silicon map is blue (representing BCB and glass), the carbon map is red and the aluminum map is white (representing the gate electrode). Now the three polymer layers can clearly be distinguished by a color code. In this way it is shown that the UV-NIL-ACMO resist is fully displaced; no residue is observed in the imprinted areas. Even bumps in the surface, indicated by the white arrow in Fig. 3c, can be identified as PVCi, thus corroborating the residue-free imprint. Despite the perfect displacement of the resist it is worth noting that both the BCB and particularly the PVCi layer seem to be compressed due to the imprint step. The influence of the compression on the electrical performance of the dielectric layers will be topic of further investigations. Furthermore, it is observed that the appearance of the resist is wedge-shaped. This is a direct consequence of the stamp’s rounded edges stemming from an isotropic etch step during the stamp fabrication. With NIL all structures of the stamp (including artifacts and defects) are strictly and precisely transferred to the resist/sample.

Since no residuals of UV-NIL-ACMO are left at imprinted areas the specimen can be covered with the source–drain electrode material without prior etching. This is particularly favorable since the dielectric layers are fairly thin and thus can easily be damaged by the etching process. The final transistor structure is shown in Fig. 4, where a scheme (Fig. 4a) and a cross section TEM image (Fig. 4b) are presented. As shown, the gold electrode is perfectly preserved in the imprinted region (right part of the image) whereas it is gone in the channel where the UV-NIL-ACMO was dissolved (left part of the image).

### 3.3. Electrical characterization of submicron OTFTs fabricated by residue-free UV-NIL

The introduced residue-free UV-NIL route obviously leads to well-defined transistor structures. Devices with channel lengths down to 700 nm were fabricated. Consequently, appropriate device characteristics are expected. The results of the $I(V)$-characterization of submicron transistors based on the 130 nm thick BCB/PVCi bilayer as the gate dielectric are shown in Fig. 5. Important parameters such as the specific gate capacitance $C_i$ and the dielectric breakdown voltage $E_{br}$ that are intrinsic to the gate dielectric are also specified in the table. The motivation for the usage of an additional ultra-thin PVCi layer forming the direct interface to pentacene is to adjust the surface energy and roughness in such a way that the semiconductor growth is optimized.

In the output characteristics (second column in Fig. 5) no difference is observed between devices with submicron channel lengths varying from 950 to 700 nm and constant W/L ratio, which is an indication for a constant charge carrier mobility $\mu$. All curves show saturation of the drain current. This is due to the fact that the gate dielectric layer thickness is smaller by more than a factor 5 than the channel length, thus preventing an unbalanced increase of the lateral electric field with respect to the vertical one. As was shown previously [11–13], an adequate downscaling of channel length and dielectric layer thickness leads to short channel effects such as channel length modulation resulting in a loss of current saturation. Moreover, at small drain voltages the drain current increases perfectly linear meaning that the transport is not limited by the contact resistance. Hysteresis effects between forward and reverse drain voltage sweeps are negligible.

From the semi-logarithmic representation of the transfer characteristics $I_D(V_G)$ in saturation (first column in Fig. 5) the subthreshold swing $S$ and the switch-on voltage $V_{so}$ were determined. The latter is taken as the gate voltage at which the drain current is one order of magnitude higher than the off-current $I_{off}$. The transfer characteristics of submicron devices for different channel lengths collapse into one curve as is expected for transistors having identical geometry (W/L ratio) and mobility. All submicron OTFTs are normally-on as is reflected by the small positive $V_{so}$ (see Fig. 5). A shift of the onset of transistor operation to the positive voltage regime was reported to be induced by negative charges in the BCB dielectric probably caused by water [23,24].

The charge carrier mobility of the UV-NIL fabricated submicron OTFTs is in the range of $10^{-3}$ cm$^2$/Vs which is
rather low compared to hot embossed submicron OTFTs with SiO$_2$ as the gate dielectric [12]. One parameter that influences the mobility and is directly related to the channel resistance is the pentacene grain size. As deduced from the AFM phase image in Fig. 2c the maximum pentacene grain size is well below 1.5 $\mu$m, which we found to be the average threshold for grain boundary limited transport [25]. If the grain size is smaller than one micron the transport is dominated by grain boundary effects. This leads to a decreased mobility in the range of $10^{-3}$ cm$^2$/V$s$ as is indeed observed in the BCB/PVC$_i$ submicron transistors. Moreover, the large amount of interface trap states that is reflected by a large subthreshold swing [26] – compared to hot embossed devices [12,13] – clearly has a negative effect on the mobility because it obstructs the charge transport by scattering carriers at the pentacene-dielectric interface. With an additional UV-ozone treatment, as described in Ref. [12], the pentacene grain size could be strongly increased both in the channel and on the contacts thus resulting in charge carrier mobilities up to 0.3 cm$^2$/V$s$ for SiO$_2$-based submicron OTFTs.

4. Conclusion

In summary, we have fabricated fully functional OTFTs with submicron channel lengths using an improved UV-NIL process. The nanoimprinted OTFTs are comprised of pentacene as active semiconductor and a thin bilayer gate dielectric composed of BCB and PVC$_i$. With our novel UV-NIL process, devices with channel lengths down to 700 nm were fabricated, showing good drain current saturation and low switch-on voltages. This process is based on a UV-NIL resist formulation containing acryloyl morpholine, which perfectly matches the requirements of fast and precise nanoimprinting of organic electronic components. Since no heating step is involved in the process, thermal stress can be disregarded and, more importantly, thermally unstable materials can be used as substrates and gate dielectrics. Furthermore, UV-NIL-ACMO is cured by UV-initiated radical polymerization which reduces the fabrication time considerably, thus enabling a high throughput. Remarkable is the absence of any residual layer of UV-NIL-ACMO after the imprint step, which makes etching obsolete. This is particularly convenient, since O$_2$-etching of organic dielectrics is known to increase the gate leakage and the number of OH-groups acting as traps at the interface. Furthermore, reactive ion etching is difficult to implement in a standard printing line. Finally, UV-NIL-ACMO allows a lift-off with deionized water, which is a substantial advantage due to its ubiquitous availability, its potential for immediate recycling and its environmental sustainability, resulting in a decrease of the production costs and an increase of process safety. Optimization is still needed with respect to the semiconductor/dielectric interface which shows an increased number of traps leading to reduced effective charge carrier mobilities after the UV-imprint step. Here, a special treatment prior to the application of the semiconductor could be beneficial and furthermore increase the pentacene grain size. In conclusion, UV-NIL has a huge potential as a high-resolution patterning process for large-area fabrication of flexible organic electronics.

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References
